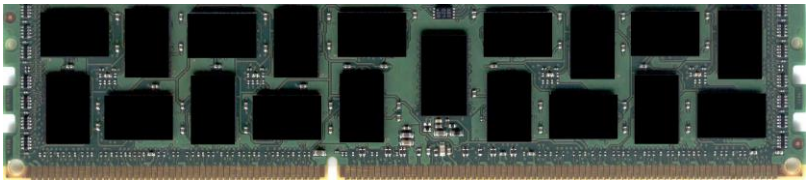
DTM64377

16GB - 240-Pin 2Rx4 Registered ECC DDR3 LV DIMM



Identification

DTM64377E 2Gx72

16GB 2Rx4 PC3L-10600-R9

Performance range

Clock / Module Speed / CL-t_{RCD} -t_{RP}
667 MHz / PC3L-10600 / 9-9-9
533 MHz / PC3L-8500 / 8-8-8
533 MHz / PC3L-8500 / 7-7-7
400 MHz / PC3L-6400 / 6-6-6

Features

- 240-pin JEDEC-compliant DIMM, 133.35 mm wide by 30 mm high
- Operating Voltage: VDD = VDDQ = +1.35V (1.283V to 1.45V)
- Backward-compatible to VDD = VDDQ = +1.5V ±0.075V
- I/O Type: SSTL_15
- On-board I^2C temperature sensor with integrated Serial Presence-Detect (SPD) EEPROM
- Data Transfer Rate: 10.6 Gigabytes/sec
- Data Bursts: 8 and burst chop 4 mode
- ZQ Calibration for Output Driver and On-Die Termination (ODT)
- Programmable ODT / Dynamic ODT during Writes
- Programmable CAS Latency: 6, 7, 8 and 9
- Bi-directional Differential Data Strobe signals
- SDRAM Addressing (Row/Col/Bank): 16/11/3
- Fully RoHS Compliant

Description

DTM64377 is a registered 2Gx72 memory module, which conforms to JEDEC's DDR3, PC3L-10600 standard. The assembly is Dual-Rank. Each Rank is comprised of eighteen 1Gbx4 DDR3L-1333 SDRAMs. One 2K-bit EEPROM is used for Serial Presence Detect and a combination register/PLL, with Address and Command Parity, is also used.

Both output driver strength and input termination impedance are programmable to maintain signal integrity on the I/O signals in a Fly-by topology. A thermal sensor accurately monitors the DIMM module and can prevent exceeding the maximum operating temperature of 95C.

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Pin Configuration

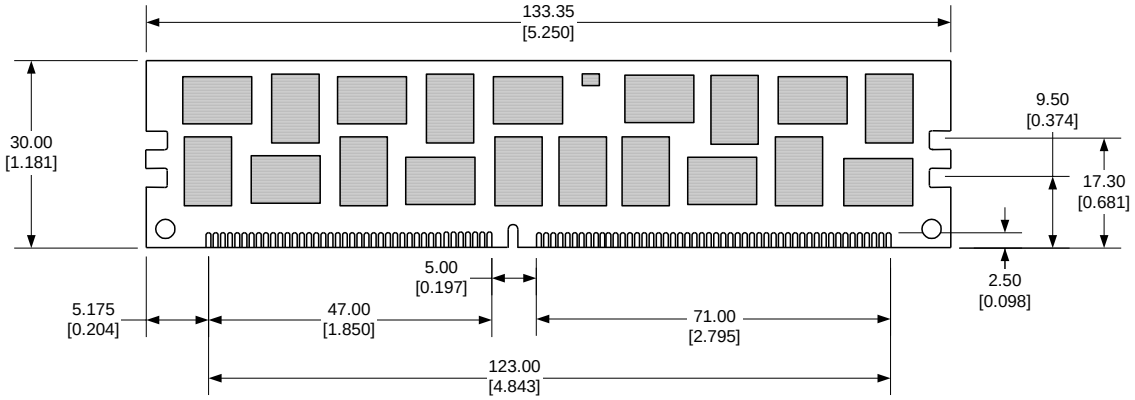
Front Side								Back Side							
1	V_{REFDQ}	31	DQ25	61	A2	91	DQ41	121	V_{SS}	151	V_{SS}	181	A1	211	V_{SS}
2	V_{SS}	32	V_{SS}	62	V_{DD}	92	V_{SS}	122	DQ4	152	DQS12	182	V_{DD}	212	DQS14
3	DQ0	33	/DQS3	63	CK1*	93	/DQS5	123	DQ5	153	/DQS12	183	V_{DD}	213	/DQS14
4	DQ1	34	DQS3	64	/CK1*	94	DQS5	124	V_{SS}	154	V_{SS}	184	CK0	214	V_{SS}
5	V_{SS}	35	V_{SS}	65	V_{DD}	95	V_{SS}	125	DQS9	155	DQ30	185	/CK0	215	DQ46
6	/DQS0	36	DQ26	66	V_{DD}	96	DQ42	126	/DQS9	156	DQ31	186	V_{DD}	216	DQ47
7	DQS0	37	DQ27	67	V_{REFCA}	97	DQ43	127	V_{SS}	157	V_{SS}	187	/EVENT	217	V_{SS}
8	V_{SS}	38	V_{SS}	68	P_{AR_IN}	98	V_{SS}	128	DQ6	158	CB4	188	A0	218	DQ52
9	DQ2	39	CB0	69	VDD	99	DQ48	129	DQ7	159	CB5	189	V_{DD}	219	DQ53
10	DQ3	40	CB1	70	A10/AP	100	DQ49	130	V_{SS}	160	V_{SS}	190	BA1	220	V_{SS}
11	V_{SS}	41	V_{SS}	71	BA0	101	V_{SS}	131	DQ12	161	DQS17	191	V_{DD}	221	DQS15
12	DQ8	42	/DQS8	72	V_{DD}	102	/DQS6	132	DQ13	162	/DQS17	192	/RAS	222	/DQS15
13	DQ9	43	DQS8	73	/WE	103	DQS6	133	V_{SS}	163	V_{SS}	193	/S0	223	V_{SS}
14	V_{SS}	44	V_{SS}	74	/CAS	104	V_{SS}	134	DQS10	164	CB6	194	V_{DD}	224	DQ54
15	/DQS1	45	CB2	75	V_{DD}	105	DQ50	135	/DQS10	165	CB7	195	ODT0	225	DQ55
16	DQS1	46	CB3	76	/S1	106	DQ51	136	V_{SS}	166	V_{SS}	196	A13	226	V_{SS}
17	V_{SS}	47	V_{SS}	77	ODT1	107	V_{SS}	137	DQ14	167	NC (TEST)	197	V_{DD}	227	DQ60
18	DQ10	48	V_{TT}	78	V_{DD}	108	DQ56	138	DQ15	168	/RESET	198	/S3, NC	228	DQ61
19	DQ11	49	V_{TT}	79	/S2, NC	109	DQ57	139	V_{SS}	169	CKE1	199	V_{SS}	229	V_{SS}
20	V_{SS}	50	CKE0	80	V_{SS}	110	V_{SS}	140	DQ20	170	V_{DD}	200	DQ36	230	DQS16
21	DQ16	51	V_{DD}	81	DQ32	111	/DQS7	141	DQ21	171	A15	201	DQ37	231	/DQS16
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	V_{SS}	172	A14	202	V_{SS}	232	V_{SS}
23	V_{SS}	53	$/E_{RR\_OUT}$	83	V_{SS}	113	V_{SS}	143	DQS11	173	V_{DD}	203	DQS13	233	DQ62
24	/DQS2	54	V_{DD}	84	/DQS4	114	DQ58	144	/DQS11	174	A12/BC	204	/DQS13	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	V_{SS}	175	A9	205	V_{SS}	235	V_{SS}
26	V_{SS}	56	A7	86	V_{SS}	116	V_{SS}	146	DQ22	176	V_{DD}	206	DQ38	236	V_{DDSPD}
27	DQ18	57	V_{DD}	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	V_{SS}	178	A6	208	V_{SS}	238	SDA
29	V_{SS}	59	A4	89	V_{SS}	119	SA2	149	DQ28	179	V_{DD}	209	DQ44	239	V_{SS}
30	DQ24	60	V_{DD}	90	DQ40	120	V_{TT}	150	DQ29	180	A3	210	DQ45	240	V_{TT}

Pin Description

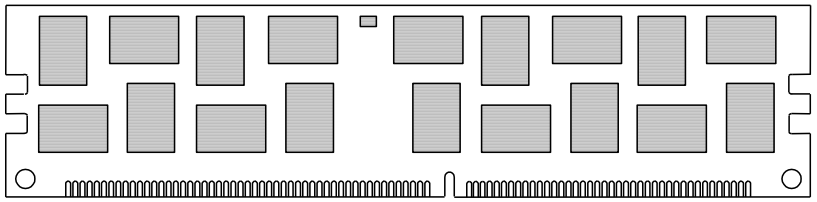
Name	Function
CB[7:0]	Data Check Bits
DQ[63:0]	Data Bits
DQS[17:0], /DQS[17:0]	Differential Data Strobes
CK[1:0], /CK[1:0]	Differential Clock Inputs
CKE[1:0]	Clock Enables
/CAS	Column Address Strobe
/RAS	Row Address Strobe
/S[3:0]	Chip Selects
/WE	Write Enable
A[15:0]	Address Inputs
BA[2:0]	Bank Addresses
ODT[1:0]	On Die Termination Inputs
SA[2:0]	SPD Address
SCL	SPD Clock Input
SDA	SPD Data Input/Output
/EVENT	Temperature Sensing
/RESET	Reset for register and DRAMs
PAR_IN	Parity bit for Addr/Ctrl
/ERR_OUT	Error bit for Parity Error
A12/BC	Combination input: Addr12/Burst Chop
A10/AP	Combination input: Addr10/Auto-precharge
V_{SS}	Ground
V_{DD}	Power
V_{DDSPD}	SPD EEPROM Power
V_{REFDQ}	Reference Voltage for DQ's
V_{REFCA}	Reference Voltage for CA
V_{TT}	Termination Voltage
NC	No Connection

*not used

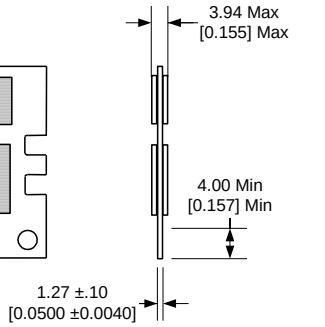
Front view



Back view



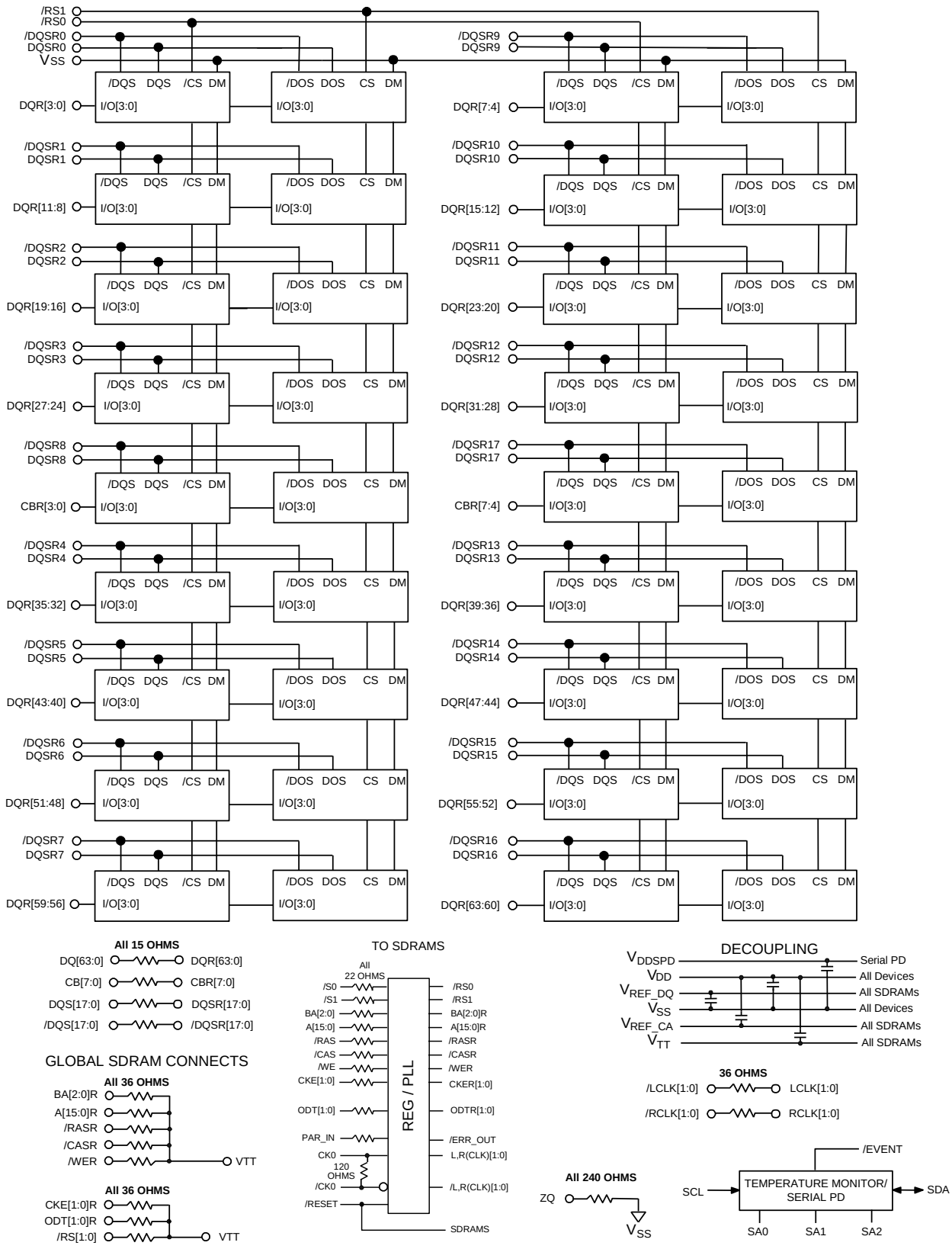
Side view



Notes

Tolerances on all dimensions except where otherwise indicated are ±.13 (.005).

All dimensions are expressed: millimeters [inches]


/RS1
/RS0
/DQSR0
DQSR0
Vss
/DQSR9
DQSR9
/DQS DQS /CS DM
/DOS DOS CS DM
I/O[3:0]
DQR[3:0]
DQR[7:4]
/DQSR1
DQSR1
/DQSR10
DQSR10
DQR[11:8]
DQR[15:12]
/DQSR2
DQSR2
/DQSR11
DQSR11
DQR[19:16]
DQR[23:20]
/DQSR3
DQSR3
/DQSR12
DQSR12
DQR[27:24]
DQR[31:28]
/DQSR8
DQSR8
/DQSR17
DQSR17
CBR[3:0]
CBR[7:4]
/DQSR4
DQSR4
/DQSR13
DQSR13
DQR[35:32]
DQR[39:36]
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/DQSR14
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DQR[55:52]
/DQSR7
DQSR7
/DQSR16
DQSR16
DQR[59:56]
DQR[63:60]
All 15 OHMS
DQ[63:0]
DQR[63:0]
CB[7:0]
CBR[7:0]
DQS[17:0]
DQSR[17:0]
/DQS[17:0]
/DQSR[17:0]
GLOBAL SDRAM CONNECTS
All 36 OHMS
BA[2:0]R
A[15:0]R
/RASR
/CASR
/WER
VTT
CKE[1:0]R
ODT[1:0]R
/RS[1:0]
TO SDRAMS
All
22 OHMS
/S0
/S1
BA[2:0]
A[15:0]
/RAS
/CAS
/WE
CKE[1:0]
ODT[1:0]
PAR_IN
CK0
120
OHMS
/CK0
/RESET
REG / PLL
/RS0
/RS1
BA[2:0]R
A[15:0]R
/RASR
/CASR
/WER
CKER[1:0]
ODTR[1:0]
/ERR_OUT
L,R(CLK)[1:0]
/L,R(CLK)[1:0]
SDRAMS
All 240 OHMS
ZQ
Vss
DECOUPLING
VDDSPD
VDD
VREF_DQ
Vss
VREF_CA
VTT
Serial PD
All Devices
All SDRAMs
All Devices
All SDRAMs
All SDRAMs
36 OHMS
/LCLK[1:0]
LCLK[1:0]
/RCLK[1:0]
RCLK[1:0]
/EVENT
SCL
TEMPERATURE MONITOR/
SERIAL PD
SDA
SA0
SA1
SA2

Absolute Maximum Ratings

(Note: Operation at or above Absolute Maximum Ratings can adversely affect module reliability.)

PARAMETER	Symbol	Minimum	Maximum	Unit
Temperature, non-Operating	$T_{STORAGE}$	-55	100	C
Ambient Temperature, Operating	T_A	0	70	C
DRAM Case Temperature, Operating	T_{CASE}	0	95	C
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-0.4	1.975	V
Voltage on Any Pin relative to V_{SS}	V_{IN},V_{OUT}	-0.4	1.975	V

Notes:

DRAM Operating Case Temperature above 85C requires 2X refresh.

Recommended DC Operating Conditions (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Operation Voltage	Minimum	Typical	Maximum	Unit	Note
Power Supply Voltage	V_{DD}	1.35V	1.283	1.35	1.4500	V	
		1.5V	1.425	1.5	1.575		
I/O Reference Voltage	V_{REFDQ}	1.35V	0.49 V_{DD}	0.50 V_{DD}	0.51 V_{DD}	V	1
		1.5V					
I/O Reference Voltage	V_{REFCA}	1.35V	0.49 V_{DD}	0.50 V_{DD}	0.51 V_{DD}	V	1
		1.5V					

Notes:

1) The value of V_{REF} is expected to equal one-half V_{DD} and to track variations in the V_{DD} DC level. Peak-to-peak noise on V_{REF} may not exceed ±1% of its DC value.

DC Input Logic Levels, Single-Ended (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Operation Voltage	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(DC)}$	1.35V	V_{REF} + 0.09	V_{DD}	V
		1.5V	V_{REF} + 0.1	V_{DD}	
Logical Low (Logic 0)	$V_{IL(DC)}$	1.35V	V_{SS}	V_{REF} - 0.09	V
		1.5V	V_{SS}	V_{REF} - 0.1	

AC Input Logic Levels, Single-Ended (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Operation Voltage	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(AC)}$	1.35V	V_{REF} + 0.160	-	V
		1.5V	V_{REF} + 0.175	-	
Logical Low (Logic 0)	$V_{IL(AC)}$	1.35V	-	V_{REF} - 0.160	V
		1.5V	-	V_{REF} - 0.175	

Differential Input Logic Levels (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Differential Input Logic High	$V_{IH.DIFF}$	+0.200	DC:V_{DD} AC:V_{DD}+0.4	V
Differential Input Logic Low	$V_{IL.DIFF}$	DC:V_{SS} AC:V_{SS}-0.4	-0.200	V
Differential Input Cross Point Voltage relative to VDD/2	V_{IX}	- 0.150	+ 0.150	V

Capacitance (T_A = 25 C, f = 100 MHz)

PARAMETER	Pin	Symbol	Minimum	Maximum	Unit
Input Capacitance, Clock	CK0, /CK0	C_{CK}	1.5	2.5	pF
Input Capacitance, Address	BA[2:0], A[15:0], /RAS, /CAS, /WE	C_I	1.5	2.5	pF
Input Capacitance Control	/S[1:0], CKE[1:0], ODT[1:0]	C_I	1.5	2.5	pF
Input/Output Capacitance	DQ[63:0], CB[7:0] DQS[17:0], /DQS[17:0].	C_{IO}	3	5	pF

DC Characteristics (T_A = 0 to 70 C, Voltage referenced to V_{ss} = 0 V)

PARAMETER	Symbol	Minimum	Maximum	Unit	Note
Input Leakage Current (Any input 0 V < VIN < VDD)	I_{IL}	-18	+18	µA	1,2
Output Leakage Current (0V < VOUT < VDDQ)	I_{OL}	-10	+10	µA	2,3

Notes:
1) All other pins not under test = 0 V
2) Values are shown per pin
3) DQ, DQS, DQS and ODT are disabled

AC Operating Conditions

PARAMETER	Symbol	Min	Max	Unit
Internal read command to first data	t_{AA}	13.125	20	ns
CAS-to-CAS Command Delay	t_{CCD}	4	-	t_{CK}
Clock High Level Width	$t_{CH(avg)}$	0.47	0.53	t_{CK}
Clock Cycle Time	t_{CK}	1.5	1.875	ns
Clock Low Level Width	$t_{CL(avg)}$	0.47	0.53	t_{CK}
Data Input Hold Time after DQS Strobe	t_{DH}	65	-	ps
DQ Input Pulse Width	t_{DIPW}	400	-	ps
DQS Output Access Time from Clock	t_{DQSCK}	-255	+255	ps
Write DQS High Level Width	t_{DQSH}	0.45	0.55	$t_{CK(avg)}$
Write DQS Low Level Width	t_{DQSL}	0.45	0.55	$t_{CK(avg)}$
DQS-Out Edge to Data-Out Edge Skew	t_{DQSQ}	-	125	ps
Data Input Setup Time Before DQS Strobe	t_{DS}	30	-	ps
DQS Falling Edge from Clock, Hold Time	t_{DSH}	0.2	-	$t_{CK(avg)}$
DQS Falling Edge to Clock, Setup Time	t_{DSS}	0.2	-	$t_{CK(avg)}$
Clock Half Period	t_{HP}	minimum of t_{CH} or t_{CL}	-	ns
Address and Command Hold Time after Clock	t_{IH}	140	-	ps
Address and Command Setup Time before Clock	t_{IS}	65	-	ps
Load Mode Command Cycle Time	t_{MRD}	4	-	t_{CK}
DQ-to-DQS Hold	t_{QH}	0.38	-	$t_{CK(avg)}$
Active-to-Precharge Time	t_{RAS}	36	$9*t_{REFI}$	ns
Active-to-Active / Auto Refresh Time	t_{RC}	49.125	-	ns
RAS-to-CAS Delay	t_{RCD}	13.125	-	ns
Average Periodic Refresh Interval 0° C $\leq T_{CASE} <$ 85° C	t_{REFI}	-	7.8	µs
Average Periodic Refresh Interval 0° C $\leq T_{CASE} <$ 95° C	t_{REFI}	-	3.9	µs
Auto Refresh Row Cycle Time	t_{RFC}	260	-	ns
Row Precharge Time	t_{RP}	13.125	-	ns
Read DQS Preamble Time	t_{RPRE}	0.9	Note-1	$t_{CK(avg)}$
Read DQS Postamble Time	t_{RPST}	0.3	Note-2	$t_{CK(avg)}$
Row Active to Row Active Delay	t_{RRD}	Max(4nCK, 6ns)	-	ns
Internal Read to Precharge Command Delay	t_{RTP}	Max(4nCK, 7.5ns)	-	ns
Write DQS Preamble Setup Time	t_{WPRE}	0.9	-	$t_{CK(avg)}$
Write DQS Postamble Time	t_{WPST}	0.3	-	$t_{CK(avg)}$
Write Recovery Time	t_{WR}	15	-	ns
Internal Write to Read Command Delay	t_{WTR}	Max(4nCK, 7.5ns)	-	ns

Notes:
1. The maximum preamble is bound by tLZDQS(min)
2. The maximum postamble is bound by tHZDQS(max)

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